NONLINEAR CIRCUIT OPTIMIZATION WITH DYNAMICALLY INTEGRATED PHYSICAL DEVICE MODELS

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ABSTRACT

The state of the art in FET circuit optimization is advanced. Our approach, which is directed at the next generation tools for yield optimization, dynamically integrates physics-based device models. We treat the Khatibzadeh and Trew FET model in a novel formulation of harmonic balance simulation. Adjoint sensitivity analysis allows efficient optimization of parameters such as device dimensions, material-related parameters, doping profile, channel thickness, etc. We demonstrate parameter extraction and power amplifier design.

INTRODUCTION

The simulation and optimization of nonlinear circuits by harmonic balance (HB) is becoming popular [1-3]. Recent developments have been devoted to the circuit level: analyses employ equivalent circuit models of the devices. Physical/geometrical/process device parameters are not generally embodied into circuit design optimization. This leaves a design gap between circuits and devices.

Here we present an approach for nonlinear circuit optimization with physics based device models *dynamically integrated* into the HB equations. Variables can include physical parameters, geometrical parameters and material-related parameters.

The physical model proposed by Khatibzadeh and Trew [4], which serves as a vehicle for our presentation, is improved by integrating the key variable V_1 into the HB equations. The restrictive condition in their algorithm is released. Their resulting double loop simulation is simplified into a single loop.

Adjoint sensitivity analysis is directly applied to physical/geometrical/process parameters, permitting powerful gradient optimization. Our work has been implemented in our research system called McCAE. The features of our approach are exposed by a parameter extraction example and a design optimization example.

DYNAMIC INTEGRATION OF PHYSICAL MODEL WITH HB SIMULATION

In nonlinear circuit optimization it is important to use a good device model. Madjar and Rosenbaum [5] proposed an analytic large-signal model for GaAs FETs. This model was improved by Khatibzadeh and Trew [4] to allow an arbitrary doping profile in the channel. It is suitable for the optimization of ion-implanted and buried channel FETs. Our work adopts the model in [4].

The model is formulated around the active region or "intrinsic" region as shown in Fig. 1. All other regions of the device are modeled using extrinsic linear elements.

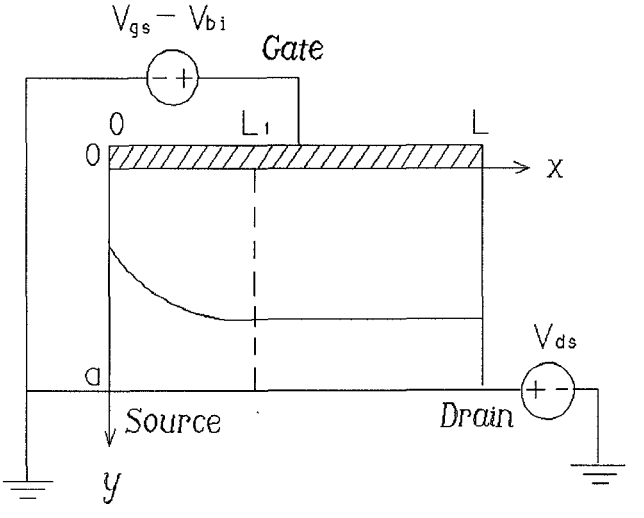

Fig. 1 Active region of the FET used in the model [4].

The output of the computer model can be represented by the equations

$$I_g = f_{Ig}(\phi, V_1, V_{gs}, V_{ds}, \partial V_{gs}/\partial t, \partial V_{ds}/\partial t) \quad (1)$$

$$I_d = f_{Id}(\phi, V_1, V_{gs}, V_{ds}, \partial V_{gs}/\partial t, \partial V_{ds}/\partial t) \quad (2)$$

$$I_s = f_{Is}(\phi, V_1, V_{gs}, V_{ds}, \partial V_{gs}/\partial t, \partial V_{ds}/\partial t) \quad (3)$$

where f_{Ig}, f_{Id} and f_{Is} are nonlinear functions, ϕ is a parameter vector including gate length, gate width, channel thickness, doping density, etc. V_{gs} and V_{ds} are gate and drain voltages in the intrinsic model.

In order to determine gate and drain currents, one must obtain the value of the intermediate variable V_1. In the original approach of [4, 5], the condition $I_d = I_s$ was used to solve for V_1, neglecting the current through the gate contact. However this condition is strictly valid for DC, and not for instan-

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taneous currents under AC excitation. Also, a double loop is required in HB simulation. The first loop is devoted to solving V_1 iteratively, then the value of V_1 is substituted into the second loop for solving the HB equations.

In our method, V_1 is integrated directly into the HB equations. For example, the HB equation for a nonlinear circuit with one FET can be written as

$$\overline{F}(\overline{V}) = \overline{Y}\begin{bmatrix}\overline{V}_{gs}\\ \overline{V}_{ds}\\ \overline{V}_1\end{bmatrix} + \overline{A}\begin{bmatrix}\overline{I}_g\\ \overline{I}_d\\ \overline{I}_s\end{bmatrix} + \overline{I}_{ss} = 0 \ , \qquad (4)$$

where a bar is used to denote the split real and imaginary parts of a complex quantity at DC, fundamental frequency and all harmonics. For example, $\overline{V}_{gs}$ is a vector containing real and imaginary parts of intrinsic gate voltage at all harmonics. $\overline{I}_g$, $\overline{I}_s$ and $\overline{I}_d$ represents the sum of conducting and displacement currents through the gate, source and drain, respectively. $\overline{Y}$ is the admittance matrix of the linear part and $\overline{A}$ is a simple incidence matrix containing 1's and 0's. $\overline{I}_{ss}$ contains excitations. Equation (4) automatically ensures the current continuity at all harmonics, i.e.,

$$\overline{I}_g + \overline{I}_s + \overline{I}_d = 0 \ . \qquad (5)$$

Therefore, our condition is valid not only for DC but also for small- or large-signal RF operation. In our approach, V_1 is allowed to vary w.r.t. time, RF input level, and operating frequency.

Our simulator needs only a single iterative loop, i.e., the loop for solving the HB equation.

SENSITIVITY ANALYSIS

Yan et al. [6] have experimented with FET performance sensitivity w.r.t. to profile and process variations. To facilitate fast gradient based iterative optimization, we have applied a recently developed adjoint sensitivity technique [7]. We first differentiate currents of the model w.r.t. voltages V_1, V_{gs} and V_{ds}. For example,

$$\partial I_g/\partial V_1 = G_{\partial Ig/\partial V1}(\phi, V_1, V_{gs}, V_{ds}, \partial V_{gs}/\partial t, \partial V_{ds}/\partial t) \ . \qquad (6)$$

The Jacobian matrix consists of such derivatives. This Jacobian is first used in the Newton update for solving the HB equations and then is reused in the adjoint equation for efficient sensitivity analysis [7].

Suppose $\overline{V}$ is a vector containing $\overline{V}_1$, $\overline{V}_{gs}$ and $\overline{V}_{ds}$. Let

$$\text{Response} = f(\phi, \overline{V}) \ . \qquad (7)$$

Here, the response can be output voltage, output current, power gain, error function for optimization, etc. Let ϕ be a generic variable such as device dimension, doping profile. The sensitivity of response w.r.t. ϕ can be computed as

$$\partial\text{Response}/\partial\phi = \partial f/\partial\phi + (\partial f/\partial\overline{V})^T(\partial\overline{V}/\partial\phi) \ , \qquad (8)$$

where $\partial f/\partial\phi$ and $(\partial f/\partial\overline{V})$ are solved analytically or by perturbation. $(\partial\overline{V}/\partial\phi)$ is calculated by adjoint sensitivity analysis.

With the dynamically integrated physical FET model and adjoint sensitivities, optimization can be applied to physical/geometrical/process parameters. We consider two examples, parameter extraction and design optimization.

PARAMETER EXTRACTION

The powerful optimization capability allows us to determine model parameters which can neither be accurately measured nor analytically derived. In our parameter extraction example, we allow the doping density, the velocity-electrical field curve, and parasitic elements to change during optimization. The objective is to best fit S-parameter measurements in the frequency range 2 to 20GHz at 3 bias points (gate bias 0V, -1.74V, -3.1V and drain bias 4V).

The model for the FET combines the extrinsic parasitic circuit and the intrinsic physical description shown in Fig. 2. The intrinsic parameters are listed in Table I. There are 16 variables and 147 nonlinear functions. It took about 30 minutes of CPU time and 13 iterations on an Apollo DN3500 to complete optimization.

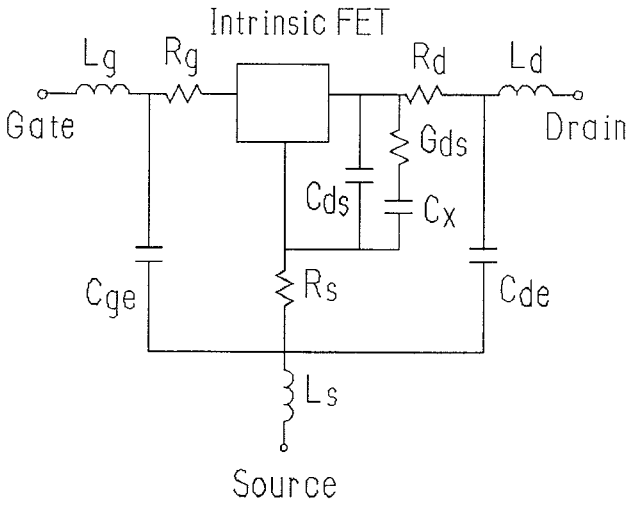

Fig. 2 Equivalent circuit showing the intrinsic FET and its associated extrinsic elements.

TABLE I

INTRINSIC PARAMETERS FOR THE MODEL [8]

Parameter	Notation	Unit
Gate Length	L	μm
Gate Width	W	μm
Channel Thickness	a	μm
Doping Density (For Uniform Doping)	N_d	cm^{-3}
Critical Electric Field	E_c	kV/cm
Saturation Velocity	v_s	cm/s
Relative Dielectric Constant	ε_r	——
Built-in Potential	V_{bi}	V
Low-Field Mobility	μ_0	$cm^2/(Vs)$
High-Field Diffusion Coefficient	D_0	cm^2/s

The values of extrinsic and intrinsic parameters extracted are listed in Table II. Fig. 3 shows the DC characteristics. A comparison between the measured and calculated S-parameters is shown in Fig. 4. Excellent agreement is obtained.

TABLE II

PARAMETER VALUES FOR THE PARAMETER EXTRACTION EXAMPLE

Intrinsic		Extrinsic	
Parameter	Value	Parameter	Value
L	0.380μm	R_g	0.027Ω
W	600μm	R_d	0.631Ω
a	0.345μm	R_s	2.428Ω
N_d	6.123×10^{16}cm^{-3}	L_g	0.146nH
E_c	3.750kV/cm	L_d	0.013nH
v_s	1.5×10^{7}cm/s	L_s	0.023nH
ε_r	12.5	G_{ds}*	
V_{bi}	0.7V	C_x	1.5pF
μ_0	4000cm^2/(Vs)	C_{ds}	2.45×10^{-6}pF
D_0	10cm^2/s	C_{ge}	0.324pF
		C_{de}	0.213pF

*G_{ds} is the bias dependent element determined by $G_{ds} = 0.00011 - 0.00097 \times V_{gs}$.

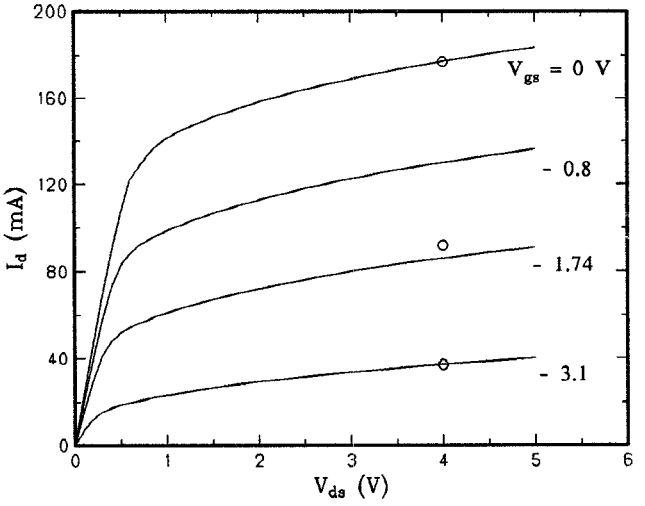

Fig. 3 DC characteristics for the parameter extraction example. The small circles indicate the measured bias points.

DESIGN OPTIMIZATION

By permitting the optimization of geometrical dimensions, material-related parameters, doping profile, etc., design optimization can be done before fabrication. A simple power amplifier example is investigated. Fig. 5 shows the amplifier schematic. It is driven by a sinusoidal generator at 2GHz with a 50Ω generator impedance and a 50Ω load. The bias conditions are -2V at the gate and 6V at the drain. Design specifications are 27dBm output power and 45% power added efficiency at 15dBm input power level. Table III lists parameters values for the FET model. The design variables include gate length L, channel thickness a, gate width W and doping density N_d.

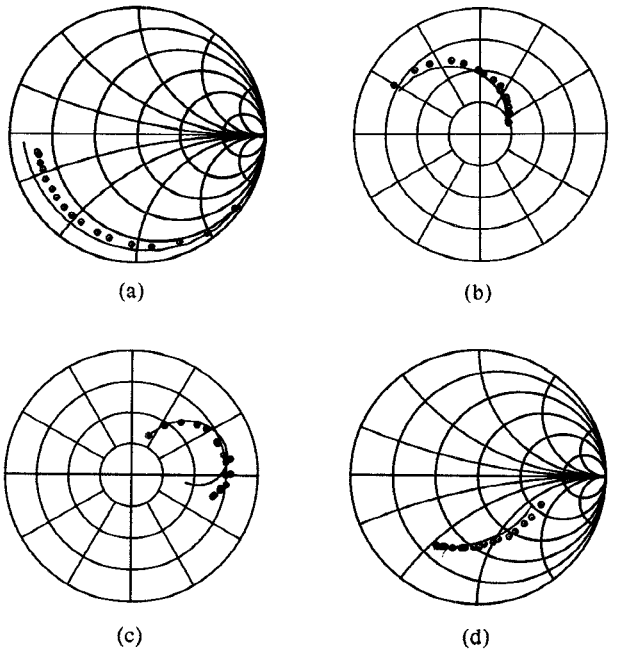

Fig. 4 Comparison of measured (circles) and calculated (solid line) scattering parameters as a function of frequency for the parameter extraction example. (a) S_{11}, (b) S_{21}, (c) S_{12} and (d) S_{22}. The gate bias is -1.74V and the drain bias is 4V.

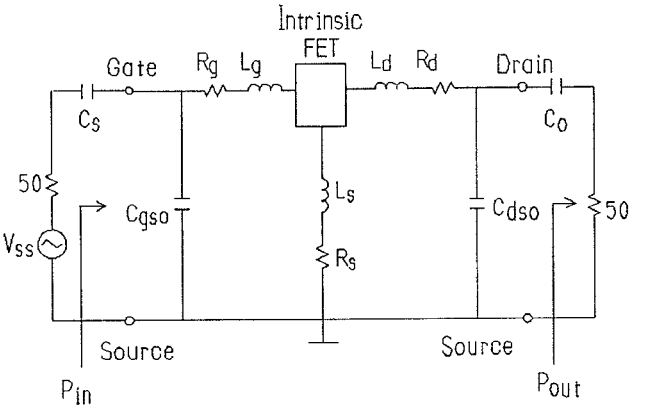

Fig. 5 A simple amplifier driven by a generator V_{SS}. C_s and C_o are the input and output capacitors, respectively. Both the generator and load impedances are 50Ω.

The starting point for optimization is

$$\phi = [L \quad a \quad W \quad N_d]^T$$

$$= [0.75\mu m \quad 0.35\mu m \quad 1200\mu m \quad 1.05\times10^{17}cm^{-3}]^T. \quad (9)$$

An efficient minimax optimization algorithm is applied to solve the design problem. The solution is

$$\phi = [0.763\mu m \quad 0.308\mu m \quad 1190\mu m \quad 9.892\times10^{16}cm^{-3}]^T.$$

TABLE III

PARAMETER VALUES FOR THE AMPLIFIER EXAMPLE BEFORE OPTIMIZATION

Intrinsic		Extrinsic	
Parameter	Value	Parameter	Value
L	0.75μm	R_g	2.6Ω
W	1200μm	R_d	0.5Ω
a	0.35μm	R_s	0.35Ω
N_d	$10.5\times10^{16}cm^{-3}$	L_g	1.1nH
E_c	3.75kV/cm	L_d	0.25nH
v_s	1.5×10^{7}cm/s	L_s	0.15nH
ε_r	12.9	C_{gso}	0.2pF
V_{bi}	0.7V	C_{dso}	0.2pF
μ_0	$4000cm^2/(Vs)$	C_o	20pF
D_0	$10cm^2/s$	C_s	20pF

The gain and power added efficiency before and after optimization are shown in Figs. 6 and 7, respectively. An improvement of 12% power added efficiency is achieved by optimization.

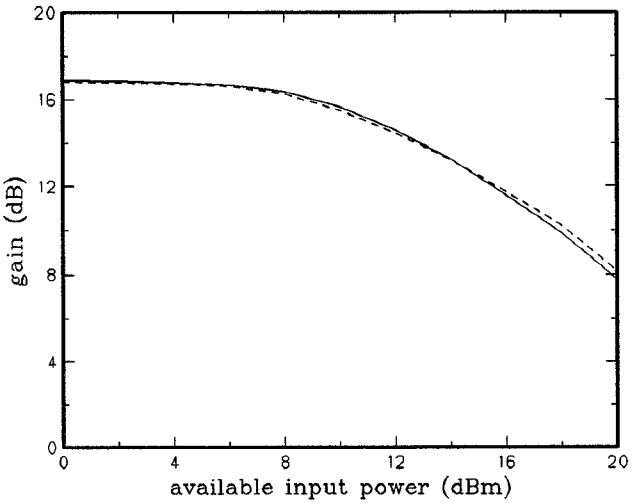

Fig. 6 Gain versus input power of the amplifier before optimization (dashed line) and after optimization (solid line).

CONCLUSIONS

Efficient harmonic balance optimization of nonlinear circuits is carried out with physics-based device models, representing a breakthrough over the conventional equivalent circuit approach. The FET model of Khatibzadeh and Trew is dynamically integrated into the HB equations, resulting in improved accuracy and efficiency. Adjoint sensitivities are analyzed directly w.r.t. physical/geometrical/process parameters. Our approach is indispensable to the inclusion of device statistics in the next generation tools for yield optimization of FET circuits and MMICs.

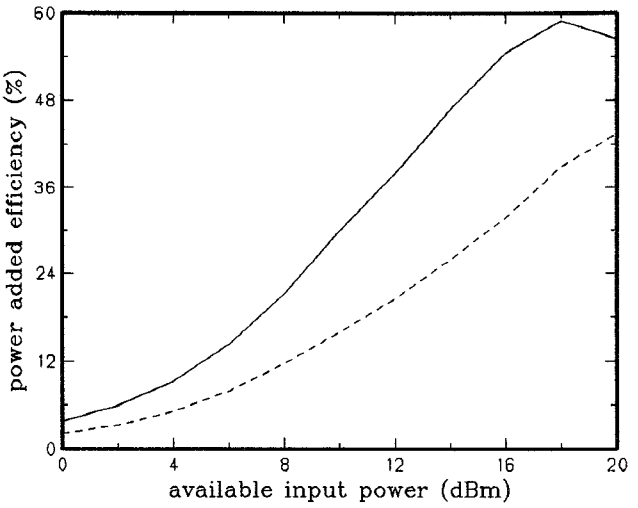

Fig. 7 Power added efficiency versus input power of the amplifier before optimization (dashed line) and after optimization (solid line).

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